IN THE CLAIMS

Claims 1-18. (Cancelled).

—19. (New) A method of automatically generating a test environment for an ATE, designed to test a single integrated circuit, the method comprising the steps of:

mapping the pins of the ATE to a plurality of integrated circuits to create pin data;

automatically generating, with a test program generator, a test program and testpattern data for the integrated circuits from pattern data, generic test program rules, and the pin data; and

executing the test program to control the ATE.--

--20. (New) The method of claim 19 further comprising the step of:

generating functional fail data for each of the integrated circuits.--

--21. (New) The method of claim 1 wherein the test program includes test vectors and pin assignments for testing the integrated circuits in parallel.--

--22. (New) An automated test system comprising:

an integrated circuit tester designed to test a single integrated circuit;

a pin data storage area capable of containing pin data for mapping a plurality of integrated circuits to the pins of the integrated circuit tester;

a generic program rules storage area; and

a test program generator capable of generating a test program from the pin data, test pattern data and generic program rules, the test program capable of controlling the integrated circuit tester for testing the integrated circuits in parallel.--

--23. (New) The automated test system of claim 22 further comprising:

a storage area capable of storing fail data generated during testing for each one of the integrated circuits.--

--24. (New) The automated test system of claim 22 wherein the test program includes test vectors and pin

assignments for testing the integrated circuits in parallel.--

--25. (New) A computer progam product comprising:

a computer usable medium having computer readable program code embodied in the medium for automatically generating a test environment for an integrated circuit tester when executed, the computer readable program code including:

computer readable program code that is capable of mapping the pins of the integrated circuit tester to a plurality of integrated circuits to create pin data; and

computer readable program code that is capable of automatically generating, with a test program generator, a test program and test pattern data fro the integrated circuits from pattern data, generic test program rules, and the pin data.